UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/528,712	09/21/2005	Richard Spitz	10191/4061	8450

26646 7590 02/01/2008

KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER	
HUBER, ROBERT T	
ART UNIT	PAPER NUMBER
4146	
MAIL DATE	DELIVERY MODE
02/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/528,712	SPITZ ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	4146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-30* is/are rejected.

7)☒ Claim(s) *16-18,22,24 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 16 -18, 22, 24, and 27 objected to because of the following informalities:

a. Regarding claim 16, the term “significantly higher” is a term of relative degree. Since no definition is given for the term "significantly higher", it is interpreted as "higher".

b. Regarding claim 16, the term “comparatively narrow” is ambiguous since no clear definition of "comparatively narrow" is given. Therefore the term "comparatively narrow" is interpreted as "narrow".

c. Regarding claim 17, the phrase “sublayers of the semiconductor system at least one of touch in a central region" is unclear, and is interpreted as "sublayers of the semiconductor system at least touch in a central region".

d. Regarding claim 18, the phrase “a dopant concentration in each of the sublayers is higher than a dopant concentration in the sublayer forming the basic substrate" is ambiguous. It is unclear if the "sublayer forming the basic substrate" is a separate sublayer, apart from the second layer, or if it is part of the second layer. A best-deemed interpretation is applied, and the "sublayer forming the basic substrate" interpreted to be part of the second layer, and "a dopant

concentration in each of the sublayers" is interpreted to be "a dopant concentration in each of the other sublayers".

e. Regarding claim 22, the term "the sawing trench" lacks antecedent basis.

f. Regarding claim 24, the term “significantly greater” is a term of relative degree. Since no explicit definition is given for the term "significantly greater", it is interpreted as "greater".

g. Regarding claim 27, the phrase “the p-n junction of the first layer with the sublayer" is ambiguous since it is unclear to which sublayer the claim is referring. A best deemed interpretation is applied, and “the p-n junction of the first layer with the sublayer” is interpreted as “the p-n junction of the first layer with either the first or second sublayer”.

Appropriate correction is required.

2. Applicant is advised that should claim 16 be found allowable, claim 28 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing

one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 16 – 19, 23, 24, and 26 – 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Kiyomura et al. (US 4,999,683).

a. Regarding claims 16 and 28, Kiyomura discloses semiconductor system having a p-n junction (e.g. figure 12), comprising a substrate having an edge region (e.g. region to the left-most of substrate 40e), which is made up of a first layer of a first conductivity type (e.g. layer 60 is p-type) and a second layer of an opposite conductivity type (e.g. layers 52, 56, and 80 are n-type), the second layer being made up of at least two sublayers (e.g. layers 52, 56, and 80), wherein

the first sublayer has a first dopant concentration (layer 62 is n+ doped),

the second sublayer (layer 56) has a second dopant concentration that is lower than the first dopant concentration (col. 4, lines 47 – 48 state that layer 62 is higher in impurity concentration than layer 56),

both sublayers together with the first layer form a p-n junction (e.g. junctions 66 and 70), the p-n junction of the first layer with the first sublayer being formed exclusively in an interior of the chip (e.g. as seen in figure 12, the p-n junction with layer 60 and layer 62 is at the interior of the chip) and the p-n junction between the first layer and the second sublayer being formed in the edge region of the chip (e.g. as seen in figure 12, the p-n junction with layer 56 and layer 60 is at the edge region),

the second layer includes a third sublayer (layer 80) having a third dopant concentration that is higher than the first dopant concentration and significantly higher than the second dopant concentration (col. 6, lines 43 - 45 discloses that layer 80 is n++ doped with a higher concentration than layers 56 and 62),

the third sublayer over a largest part of its cross-sectional area in the interior of the semiconductor system borders immediately on the first sublayer (e.g. as seen in figure 12, layer 80 borders a largest part with layer 62), while bordering on the second sublayer only in a comparatively narrow edge region of the cross-sectional area (e.g. as seen in figure 12, layer 80 borders on a narrow edge with layer 56).

b. Regarding claim 17, Kiyomura discloses the semiconductor system of claim 16, as cited above, wherein the sublayers of the semiconductor system at least touch in a central region of the semiconductor system, and overlap in

regions (e.g. figure 12 shows the sublayers 56, 62, and 80 touching in a central region and overlapping).

c. Regarding claim 18, Kiyomura discloses the semiconductor system of claim 16, as cited above, wherein a dopant concentration in each of the sublayers is higher than a dopant concentration in the sublayer forming the basic substrate. (e.g. Col. 4, lines 33 – 34 and 47 - 48, and col. 6, lines 43 – 45, disclose the dopant concentration of layers 62 and 80 are higher than the substrate layer 56).

d. Regarding claim 19, Kiyomura discloses the semiconductor system of claim 16, as cited above, wherein in its central region the sublayers form a first p-n junction between a p+-doped and an n+-doped semiconductor substrate (e.g. figure 12, junction 70).

e. Regarding claim 23, Kiyomura discloses the semiconductor system of claim 16, as cited above, wherein the semiconductor system is part of a diode (col. 6, line 27 discloses the invention to be a Zener diode).

f. Regarding claim 24, Kiyomura discloses the semiconductor system of claim 16, as cited above, wherein a breakdown voltage in the edge region of the semiconductor system is significantly greater than a breakdown voltage in a

central region of the semiconductor system (col. 6, line 66, - col. 1, line 4, disclose the breakdown to occur in the layer 62, which is in the center region, due to the highest field strength in that region).

g. Regarding claim 26, Kiyomura discloses the semiconductor system of claim 16, as cited above, wherein a bulk resistance in a central region of the semiconductor system is lower than the bulk resistance in an edge region of the semiconductor (e.g. col. 7, lines 6 - 19, disclose that the reverse current flows through the layers 60, 62, and 80 due to a path of lower resistance).

h. Regarding claim 27, Kiyomura discloses a semiconductor system having a p-n junction (e.g. figure 12), comprising a substrate having an edge region (e.g. region to the left-most of substrate 40e), which is made up of a first layer of a first conductivity type (e.g. layer 60 is p-type) and a second layer of an opposite conductivity type (e.g. layers 52, 56, and 80 are n-type), the second layer being made up of at least two sublayers (e.g. layers 52, 56, and 80),

the first sublayer having a first dopant concentration (layer 62 is n+ doped) and

the second sublayer (layer 56) having a second dopant concentration that is lower than the first dopant concentration (col. 4, lines 47 – 48 state that layer 62 is higher in impurity concentration than layer 56),

both sublayers together with the first layer forming a p-n junction (e.g. junctions 66 and 70), the p-n junction of the first layer with the sublayer being formed exclusively in an interior of the chip (e.g. as seen in figure 12, the p-n junction with layer 60 and layer 62 is at the interior of the chip) and a p-n junction between the first layer and the second sublayer being formed in an edge region of the chip (e.g. as seen in figure 6, the p-n junction with layer 56 and layer 60 is at the edge region),

wherein a layer over a largest part of a cross-sectional area in the interior of the semiconductor system borders immediately on the first layer (e.g. as seen in figure 12, layer 80 borders a largest part with layer 62), while bordering on the second layer only in a comparatively narrow edge region of the cross-sectional area (e.g. as seen in figure 12, layer 80 borders on a narrow edge with layer 56).

i. Regarding claim 29, Kiyomura discloses a method for manufacturing a semiconductor system (e.g. as seen in figure 12), comprising

manufacturing a semiconductor substrate of a first conductivity type forming a first sublayer (sublayer 56) of the semiconductor system;

doping the first sublayer on both sides for forming two further sublayers of the same conductivity type as the first sublayer but with different degrees of doping (sublayers 62) so that the two sublayers touch or overlap at most in a central region of the semiconductor system (e.g. as seen in figure 12);

producing a fourth sublayer of an opposite conductivity type by introducing a dopant into the sublayers and by increasing the dopant concentration of the sublayer (e.g. layer 60, disclosed in col. 4, lines 56 – 65);

covering outer surfaces of the sublayers with metallic contact layers (layers 48 and 52, disclosed in col. 4, lines 31 – 32);

wherein the semiconductor system has a p-n junction (e.g. as seen in figure 12), including a substrate having an edge region (e.g. region to the left-most of substrate 40e), which is made up of the first layer of a first conductivity type (e.g. layer 60 is p-type) and a second layer of an opposite conductivity type (e.g. layers 52, 56, and 80 are n-type), the second layer being made up of at least two sublayers (e.g. layers 52, 56, and 80),

wherein the first sublayer has a first dopant concentration (layer 62 is n+ doped),

the second sublayer (layer 56) has a second dopant concentration that is lower than the first dopant concentration (col. 4, lines 47 – 48 state that layer 62 is higher in impurity concentration than layer 56,

both sublayers together with the first layer form a p-n junction (e.g. junctions 66 and 70), the p-n junction of the first layer with the first sublayer being formed exclusively in an interior of the chip (e.g. as seen in figure 12, the p-n junction with layer 60 and layer 62 is at the interior of the chip) and the p-n junction between the first layer and the second sublayer being formed in the

edge region of the chip (e.g. as seen in figure 12, the p-n junction with layer 56 and layer 60 is at the edge region),

the second layer includes a third sublayer (layer 80) having a third dopant concentration that is higher than the first dopant concentration and significantly higher than the second dopant concentration (col. 6, lines 43 - 45 discloses that layer 80 is n++ doped with a higher concentration than layers 56 and 62),

the third sublayer over a largest part of its cross-sectional area in the interior of the semiconductor system borders immediately on the first sublayer (e.g. as seen in figure 12, layer 80 borders a largest part with layer 62), while bordering on the second sublayer only in a comparatively narrow edge region of the cross-sectional area (e.g. as seen in figure 12, layer 80 borders on a narrow edge with layer 56).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyomura in view of Andoh (US 2002/0127890 A1). Kiyomura discloses the semiconductor system as applied to claim 16 above, however Kiyomura is silent with respect to the edge region the sublayers form a second p-n junction between a p+-doped and an n--

doped semiconductor substrate. Andoh teaches that a semiconductor system (figure 2) may contain sublayers that form p-n junctions (junction layer 18) between a p+-doped (layer 13) and a n- -doped (layer 15) semiconductor substrate.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kiyomura such that a sublayer is n- -doped, as taught by Andoh. One would have been motivated to make such a modification since lightly doping the substrate will yield desirable electrical characteristics region of the p-n junction, such as a slightly increased conductivity and reduced breakdown voltage.

7. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyomura in view of Goebel et al. (US 6,716,714 B1).

a. Regarding claim 21, Kiyomura discloses the semiconductor system of claim 16, as cited above, wherein it has in its edge region a wide, shallow sawing trench having a sawing width and a sawing depth (e.g. figure 12, regions in layer 46 at the edge of the semiconductor 40e above the P+ regions). Kiyomura is silent with respect to the sawing width being at least one of greater than 80 micrometers and 100 micrometers, and a ratio of the sawing width to the sawing depth has a value greater than 3. Goebel discloses sawing widths of approximately 40 – 150 micrometers on the edge of diodes (col. 3, lines 29 - 30), but is silent with respect to a width to depth ratio.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the side trenches of the semiconductor system of Kiyomura, in view of the trench widths as taught by Goebel, to have a certain width and depth ratio, since it has been held by the courts that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device, and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. *In Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984). One would be motivated to make a trench width of 80 - 150 micrometers since would have been a typical width of a sawing blade that produces trenches, as disclosed by Goebel. One would further be motivated to have a depth, and hence a width-to-depth ratio, in a certain range so that the cut does not go all the way through the substrate, but still is deep enough to create a trench that delineates and separates the diodes on the semiconductor substrate.

b. Regarding claim 22, Kiyomura discloses the semiconductor system of claim 16, as cited above, but is silent with respect to the sawing trench completely filled with solder material so that the wall surfaces of the sawing trench are covered by solder material and are protected by this solder material.

Goebel discloses that trenches of semiconductor devices may be filled with solder material (col. 2, lines 14 – 18).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the semiconductor system of Kiyomura to include trenches fill with solder since it was known in the art to make such modifications to semiconductor devices, as taught by Goebel. One would be motivated to make such modification because trenches filled with solder in semiconductor devices thermally couple the semiconductor device and helps to dissipate heat, keeping the device cooler.

8. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyomura. Kiyomura discloses the semiconductor system of claim 24, as cited above. However Kiyomura is silent with respect to explicitly disclosing that the breakdown voltage in the edge region is greater than the breakdown voltage approximately by a factor of 2 to 7.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to have a breakdown voltage in the edge region that is greater than the breakdown voltage by approximately a factor of 2 – 7 since Kiyomura discloses the structural limitations of the semiconductor device. It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233. One would be motivated to have a breakdown voltage in the edge region that is greater than

the breakdown voltage by a factor of 2 - 7 since a larger breakdown voltage range in the edge region would create a pathway in regions other than the edge. Since the breakdown voltage is dependent on the doping of the semiconductor, a breakdown voltage range in the edge that is greater than the other regions by a factor of 2 – 7 can be achieved while still maintaining semiconductor diode processing of the edge region and other regions that are efficient and within the scope of reasonable, known methods at the time the invention was made.

9. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyomura. Kiyomura discloses the semiconductor system of claim 16, as cited above, but is silent with respect to the p-doped and n-doped layers being interchanged.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Kiyomura and interchange the p-doped and n-doped layers, since it is well-known in the art that p-type and n-type doping are complimentary semiconductor doping methods, and that it is common and well-known in the art to interchange the dopants. One would be motivated to make such a modification since the underlying substrate may be purchased either p-doped or n-doped, and the ability to dope the substrate with either n-type or p-type dopant would increase flexibility with production.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (8am - 5pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marvin Lateef can be reached on (571) 272-5026. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 4146
January 28, 2008

/Marvin M. Lateef/
Supervisory Patent Examiner, Art Unit 4146